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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,808	06/22/2006	**Rohini Krishnan**	NL03 1474 US1	6873

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EXAMINER	
WHITE, DYLAN C	
ART UNIT	**PAPER NUMBER**
2819	

NOTIFICATION DATE	DELIVERY MODE
03/04/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,808	KRISHNAN ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 7-21* is/are pending in the application.

4a) Of the above claim(s) *3,5 and 6* is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4,7-11 and 15-21* is/are allowed.

6)☒ Claim(s) *12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Examiner acknowledges the applicants amendments to claim 1, 2, 4, and 7-12, as well as the addition of new claim 15-21. Claims 3, 5 and 6 have been cancelled during prosecution.

Response to Arguments

Applicant's arguments filed 11/8/2009 have been fully considered but they are not persuasive. The arguments with respect to claim 12 have been considered but are not persuasive over the prior art reference of Song. An explanation as well as rejection of the claims will follow in this Office Action

Regarding claim 12 the applicant argues several points with respect to the cited prior art reference of Song.

First the applicant purports that the Examiner deliberately ignored limitation of the claims. The Examiner strongly disagrees with the applicants assertion and directs the application to next time point out exactly which limitation the Examiner was deliberately ignoring in the rejection of the claims. Furthermore the Examiner was attempting to tell the applicant that several of the claims are broad enough to be read in light of several different references. No references were disclosed but the Examiner was only trying to let the applicant know that his claims are too broad, as it was the 5th official

correspondence from the PTO. The Examiners argument in response the applicants arguments is not taken as "prior art" and the language used by the examiner, for example the use of the term "simply" does not imply that the Examiner is ignoring limitations. It was only used to describe the overall basic concept of the circuit which is well known in the art.

The Examiner points out that the Applicant takes issue with the Examiners broadest reasonable interpretation of the claim language stating that it has to be consistent with the specification as well as those of ordinary skill in the art. The Examines broadest reasonable interpretation must be understood to one of ordinary skill in the art but does not have to rely of the description from the specification especially where the structure of components is often different or where knowledge is well known in the art.

Regarding claim 12, the Applicant argues that Song does not disclose having different fan-in or fan-out capabilities. The Examiner strongly disagrees with this argument for several reasons. First, the term fan-in and fan-out is usually used to describe the ability of a logic gate to support a number of other logic gates at the input and/or output of the logic circuit. Fro example a circuit with a single input from another logic circuit has a fan in of one. Fan out is different if the fact that it is determined by the number of logic circuits that can be coupled to a single output before the output can no longer sent a quality and reliable signal to the other circuits it is connected to. In the

direct case Song's disclosed circuit inherently has a fan in depending on what is being considered an input to the circuit. Furthermore the circuit has some fan out ability in which the output will degrade when too many other circuits are coupled to the output. Therefore despite the fact that Song does not directly disclose fan-in and fan-out the circuit inherently has both fan-in and fan-out capabilities. Furthermore, as the output array 105 turns on and off transistors to adjust the overall impedance of the array the current supplied to pad (101) is either increased or decreased. Because fan out is based on current flow and the amount of current the circuit can supply to other circuits coupled to the output as the current flow increases the fan out potential increases and as it current flow decreases the fan out potential decreases. Therefore the circuit os Song has the ability to change the fan out based on the current flow of array 105.

Next, the Applicant argues that Song fails to disclose switching off a buffer circuit. The Examiner respectfully disagrees with the Applicant on this argument. A buffer is a circuit that buffers a signal in some manner. There are several circuit arrangements which can constitute a buffer circuit and need only buffer a signal in some way. In the direct case the examiner is using pairs of P and N channel transistors in the output array 105. MP1 and MN1 which are connected in series between a power (VDDQ) and a ground (VSSQ) nodes with inputs UP1 and DN1 can constitute a buffer circuit as it is buffering a signal on pad (101). One of ordinary skill in the art would understand that a pair of transistors connected in this manner can constitute a buffer circuits.

The Applicant further argues that the transistor pairs of Song should not be considered a buffer because they do not buffer or store a signal. The Examiner respectfully disagrees with the applicants. First the any of the pairs of transistors in the array 105 together constitute a buffer circuit as they buffer a signal on pas (101). Furthermore, a buffer does not have to in any way store a signal. The Examiner points out that there are buffers (such as telecommunication buffers) which do store information but the storing of information is not a limitation of the term buffer and therefore a circuit does not have to store information to be considered a buffer.

Relating to the previous argument the applicant does not believe that a buffer can be turned off because there are no buffers that store or buffer the signal. The Examiner disagrees with the applicant and points to array 105 where the transistors of the array, which can constitute buffers when in pairs, can be turned on of off with the control signal at the gate of the transistors. The control signals at the gate of the transistors is from the output of the counter circuits when control when the transistors are turned on of off. When the transistor pairs are turned off then the buffer is turned off and when any of the transistors of the array 105 are turned off then it is operating at less than a maximum drive capacity.

Lastly the applicant argues that Song does not disclose a delay specification. The Examiner disagrees because the term delay specification is broad and can be any one of a number of delays within a circuit. A delay specification could be the overall

delay of the circuit from when a signal is input until the output is stable. Or the delay might be such that the circuit only needs to be faster than the maximum propagation delay allowed in the overall circuit. Therefore just claiming a delay specification does not specify exactly where or what the delay specification is pertaining to or a result of.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Song (U.S. Pat. 6,836,143)

Regarding claim 12, Song discloses determining a load (203 & 204 @ Fig. 3) applied to at least one circuit component (pad 106) having different fan-in or fan-out (element 106 has a fan in of 1) depending on a configuration of the configurable circuit (107) arrangement; and switching off a buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect. @ Fig. 2A) connected to the configurable circuit (107) according to the determination of the applied load (via comparators 203 & 204), wherein switching off the buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect. @ Fig. 2A) adjusts a drive capacity (strength of the array of output buffers 105) of the at least one circuit component (105) responsive to the determination step (comparators 203 & 204) to a value less than a maximum drive capacity (when at least one buffer (transistor pair of

array 105)) while still meeting a delay requirement (propagation delay from measuring the load to updating the output array).

Regarding claim 13, Song discloses further comprising simultaneously switching off a section of buffers (both controls signals are generated at the same time when the counters are clocked).

Regarding claim 14, Song discloses deriving the control signal (UP [i:0] and DOWN [i:0]) from a most significant bit of a selection signal (output of comparator).

Allowable Subject Matter

Claims 1, 2, 4, 7-11 and 15-21 are allowed. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, A configurable circuit arrangement comprising ***at least one circuit component at which a load is applied that can vary during operation of said circuit arrangement***, wherein said configurable circuit arrangement comprises: ***load determination means for determining a load applied at said at least one circuit component*** having different fan-in or fan-out depending on a configuration of said configurable circuit arrangement; and adjusting means for switching off a buffer connected to the at least one circuit component according to the determination of the applied load, wherein switching off the buffer adjusts a drive capacity of said at least

one circuit component to a value less than a maximum drive capacity while still meeting a delay specification.

Regarding claims 2, 4, 7-11, as being dependent on claim 1.

Regarding claim 15, A configurable circuit arrangement comprising: ***at least one circuit component at which a load is applied that can vary during operation of said configurable circuit arrangement***; load determination means for determining a load applied at said at least one circuit component, wherein the at least one circuit component has different fan-in or fan- out depending on a configuration of said configurable circuit arrangement, ***wherein said determination means is configured to determine said load based on a configuration information loaded to said configurable circuit arrangement, wherein said configuration information is stored in a configuration memory***; and adjusting means for switching off a buffer connected to the at least one circuit component according to the determination of the applied load, wherein switching off the buffer adjusts a drive capacity of said at least one circuit component to a value less than a maximum drive capacity while still meeting a delay specification.

Regarding claims 16-21, as being dependent on claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to output buffer circuitry and load determination.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819